CLASS 8&9

STABILITY OF BJT BIASING CIRCUITS, BJT AS A SWITCH, SMALL-SIGNAL EQUIVALENT CIRCUIT OF THE BJT AND FETs

PARAMETERS THAT CAN CHANGE THE Q-POINT

- **The DC current gain of the CE, β_{DC} or h_{FE} , for one type of transistor is typically available in a large range, h_{FE} = 50 to 300. The large range of β_{DC} or h_{FE} influences the transistor's biasing as**

  $I_C = \beta_{DC} I_B$ (if the leakage current is neglected).

  If I_B is fixed and β_{DC} is varied, I_C will also change.

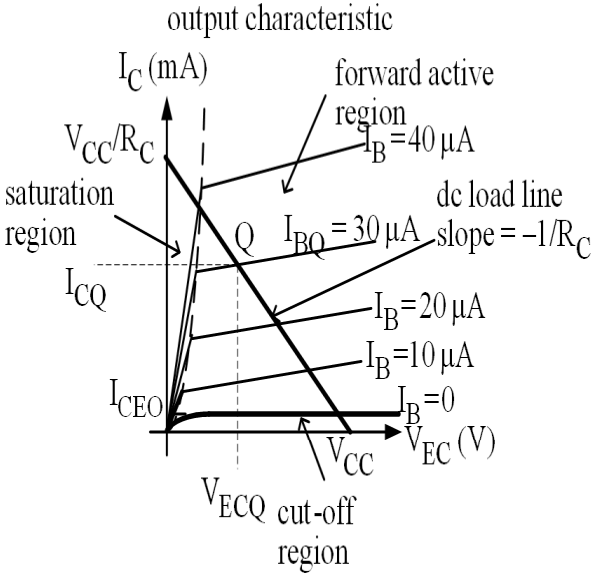
  I_{CQ} and V_{CEQ} will change, i.e. the operating point changes.

  The transistor might not be operating in the active region.

- **Temperature can also change the operating point as the temperature changes the number of minority carriers. This can be seen from the expressions:**

  $I_C = \beta_{DC} I_B + I_{CEO} = \alpha_o I_E + I_{CBO}$

  where the I_{CEO} and I_{CBO} are the minority carrier currents.



- **The dc load line can be determined by analyzing the transistor's circuit.**
- **The transistor load line is linear and is in the form:**

  $y = mx + c$

  By looking at the output characteristic of the CE,

  $y = I_C$

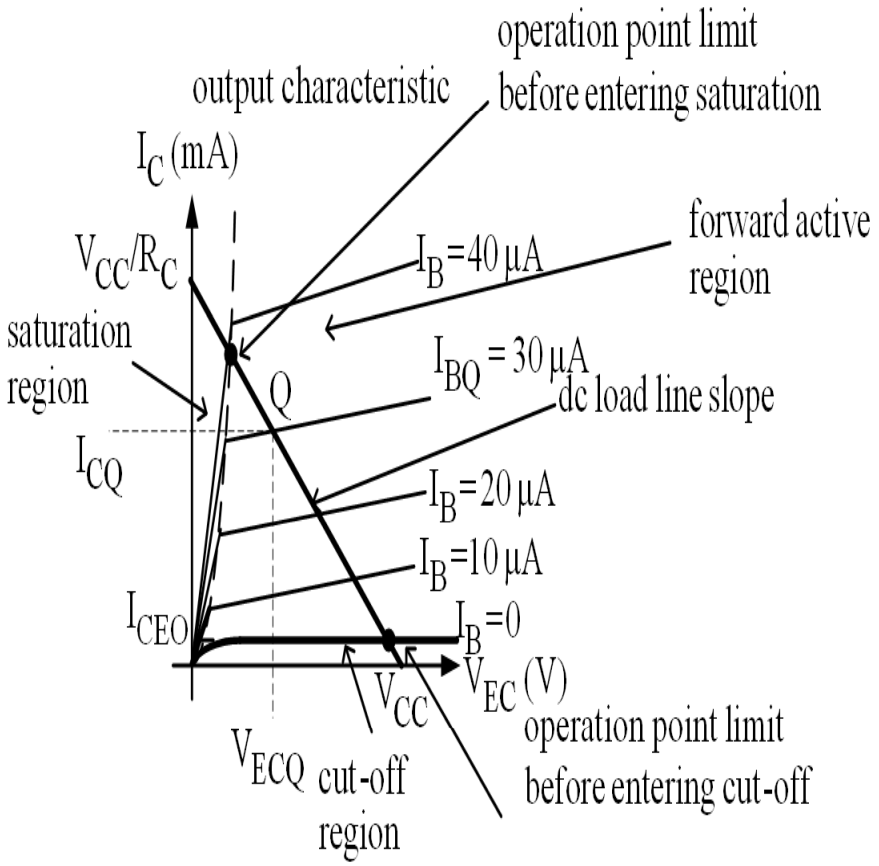
  $x = V_{EC}$

  m = slope of the load line

  c = intersection of the load line with the I_C axis.

  The load line intersects the V_{EC} axis at $I_C = 0$.

- **When I_{BQ} is known, the value of I_{CQ} and V_{ECQ} can be determined by the intersection of the dc load line with the I_{BQ} curve.**



$V_{EC} + I_C R_C - V_{CC} = 0$

$y = mx + c$

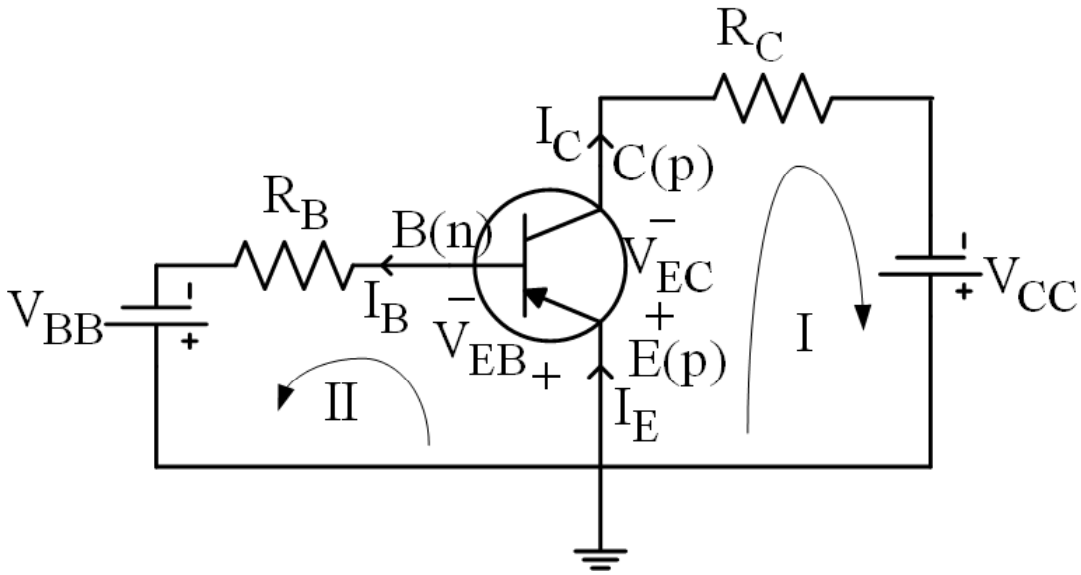
$y = I_C$, $x = V_{EC}$

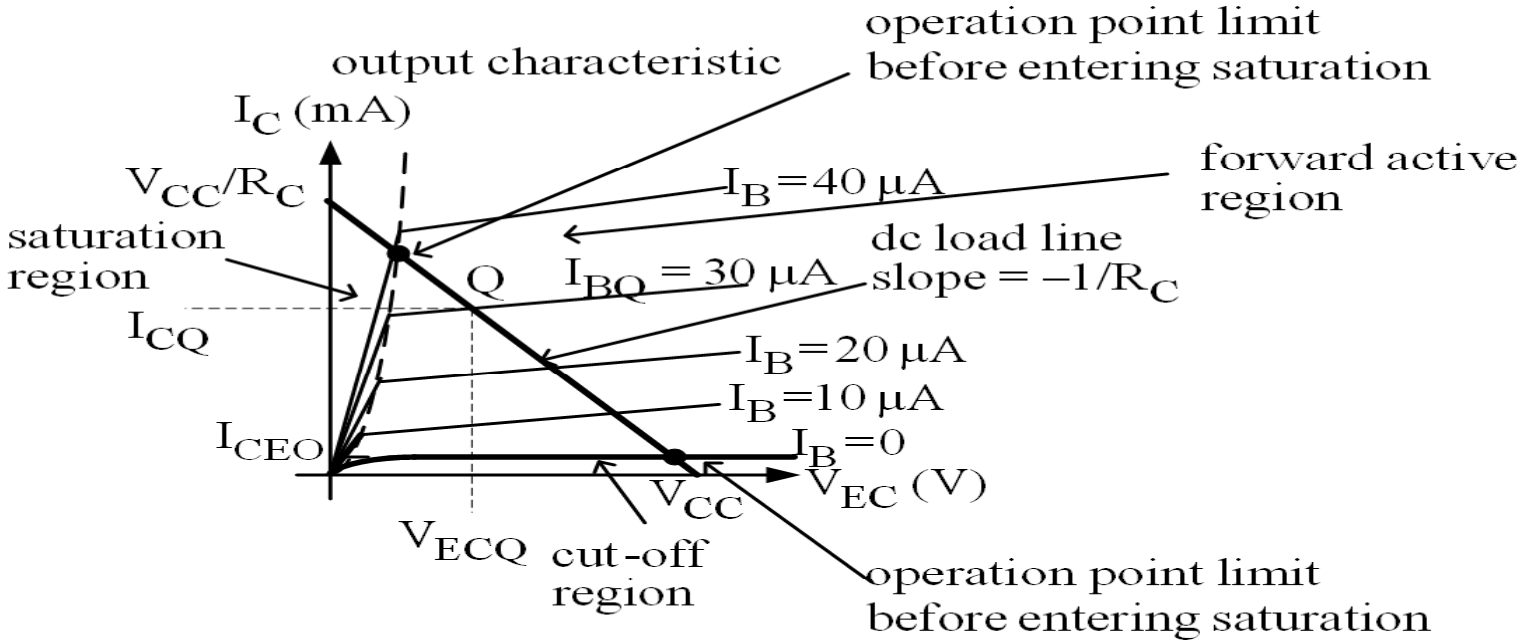
$I_C = - V_{EC} / R_C + V_{CC} / R_C$

$m = - 1 / R_C$, $c = V_{CC} / R_C$

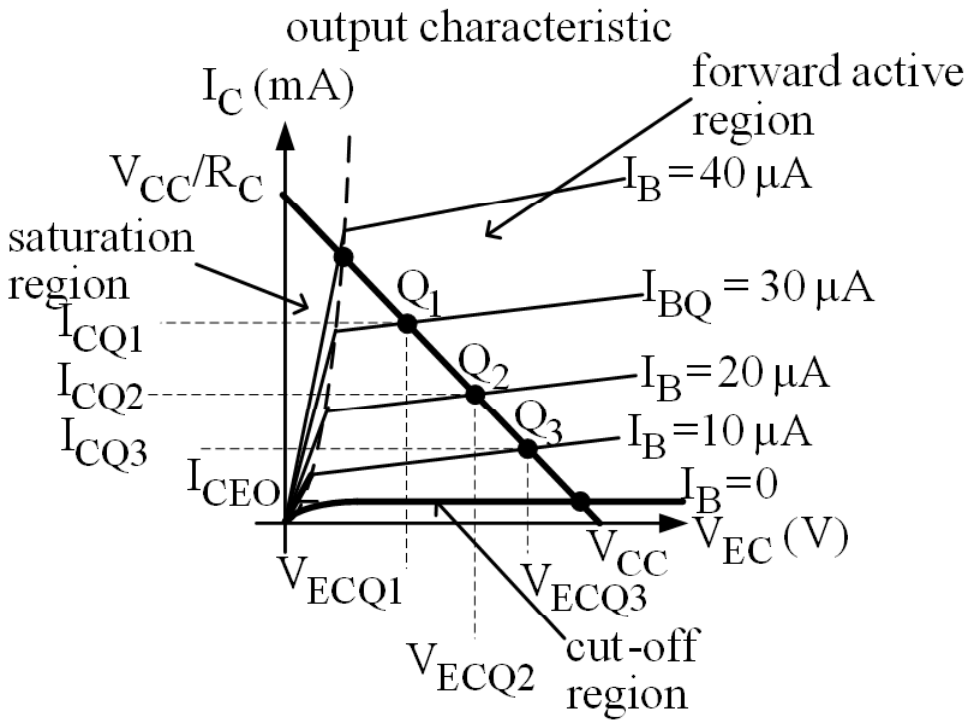
When $I_C = 0$, $V_{EC} = V_{CC}$.

When $V_{EC} = 0$, $I_C = V_{CC} / R_C$





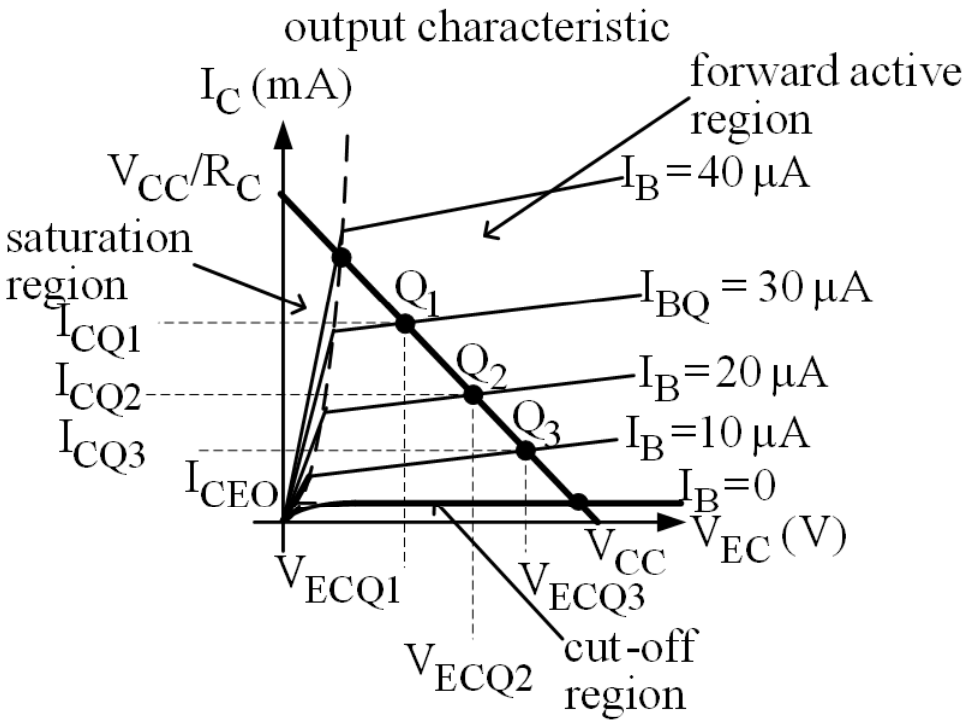
- **If the quiescent B current is I_{BQ}, then the operation point is Q_1 with output C current, I_{CQ1}, and E-C voltage, V_{ECQ1}.**
- **If the quiescent B current is 20 μA, then the operation point is Q_2 with output C current, I_{CQ2}, and E-C voltage, V_{ECQ2}.**
- **If the quiescent B current is 10 μA, then the operation point is Q_3 with output C current, I_{CQ3}, and E-C voltage, V_{ECQ3}.**



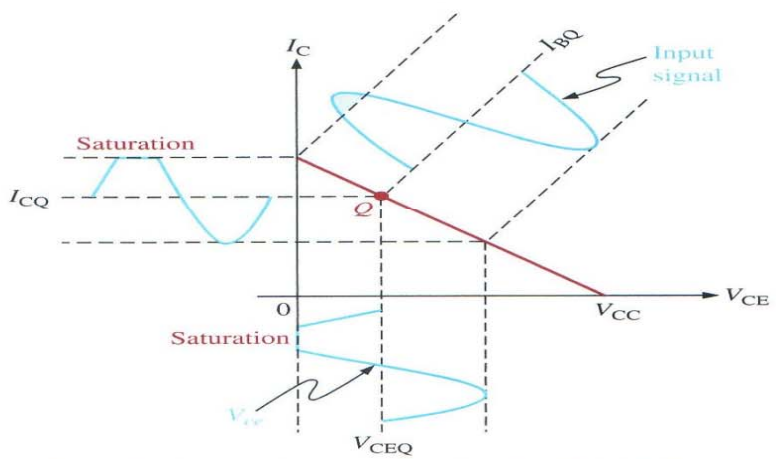
If inaccurate Q is chosen:

- **Transistor can be driven into saturation region (if Q is too close to the saturation region)**
- **Transistor can be driven into cut-off region (if Q is too close to the cut-off region)**
- **Transistor can be driven into both saturation and cut-off region (the Q point might be at the centre but the signal is too large)**

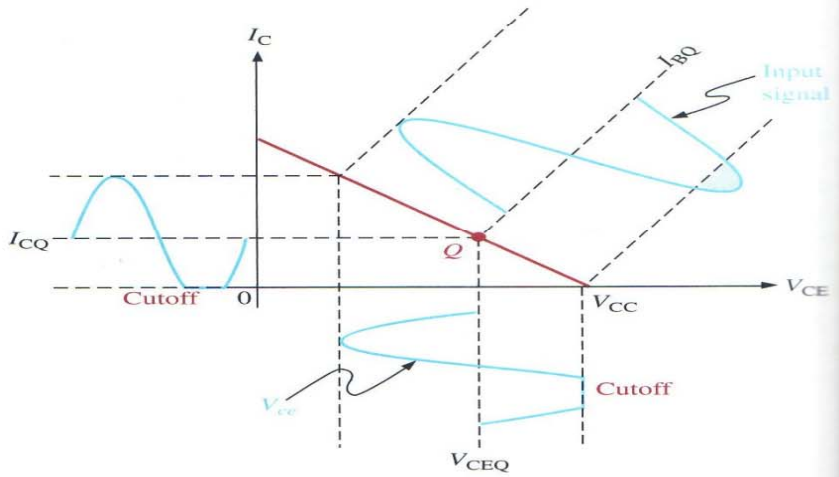
The result is a distorted signal at the output. This defeats the purpose of using the amplifier which is to have an amplified replica of the input signal at the output.



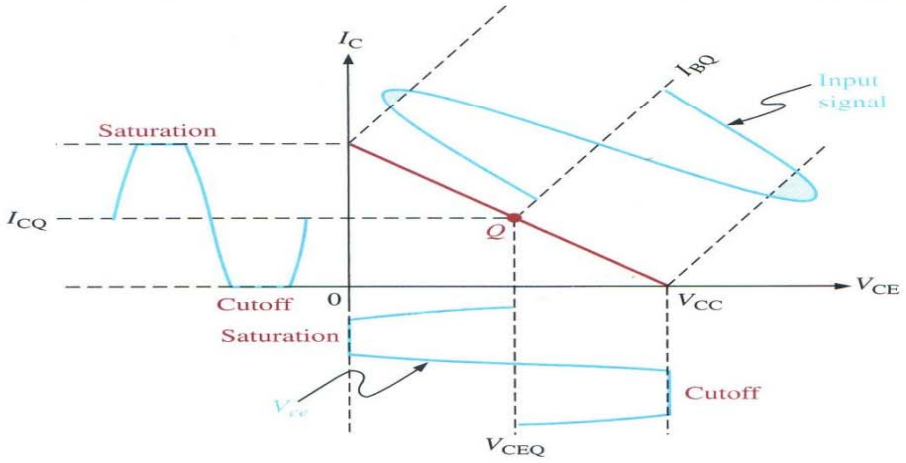
From Floyd, Electronic Devices, Sixth Edition.



(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.



(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.



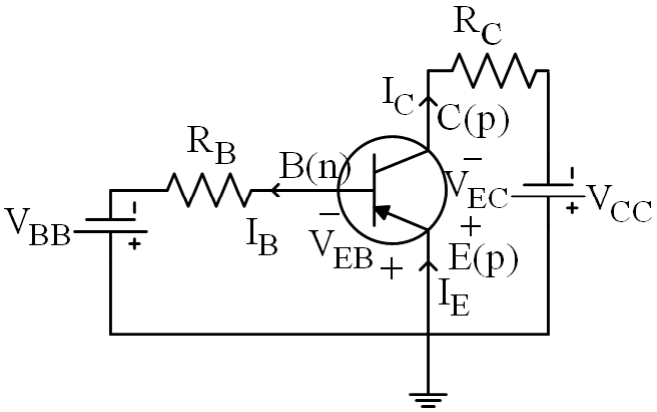
(c) Transistor is driven into both saturation and cutoff because the input signal is too large.

FIGURE 5–6

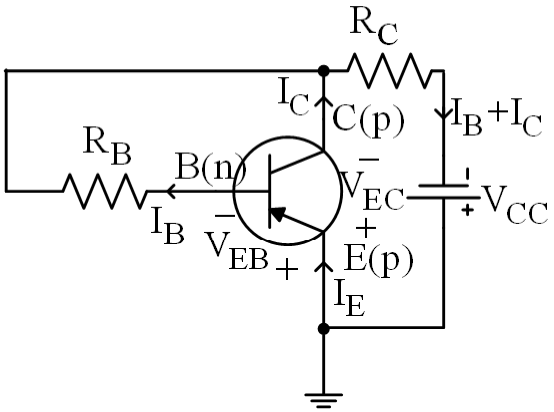
Graphical load line illustration of a transistor being driven into saturation and/or cutoff.

DC BIASING CIRCUITS

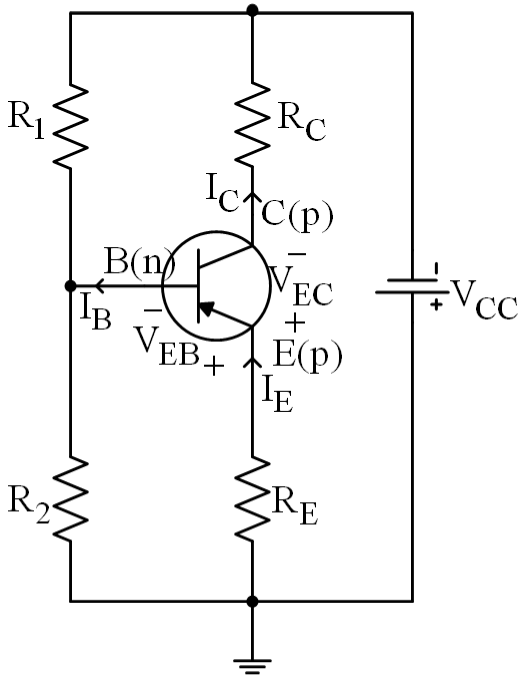
1. **Fixed-current/Base biasing circuit - Unstable**
2. **Collector-Base/Collector feedback biasing circuit - Stable**
3. **Voltage division biasing circuit - Stable and the most popular**



1. Fixed-current/Base biasing circuit



2. Collector to Base /Collector feedback biasing circuit



3. Voltage division biasing circuit

FIXED-CURRENT / BASE BIASING CIRCUIT

KVL for loop I:

$V_{EC} + I_C R_C - V_{CC} = 0$

$V_{EC} + I_C R_C = V_{CC}$

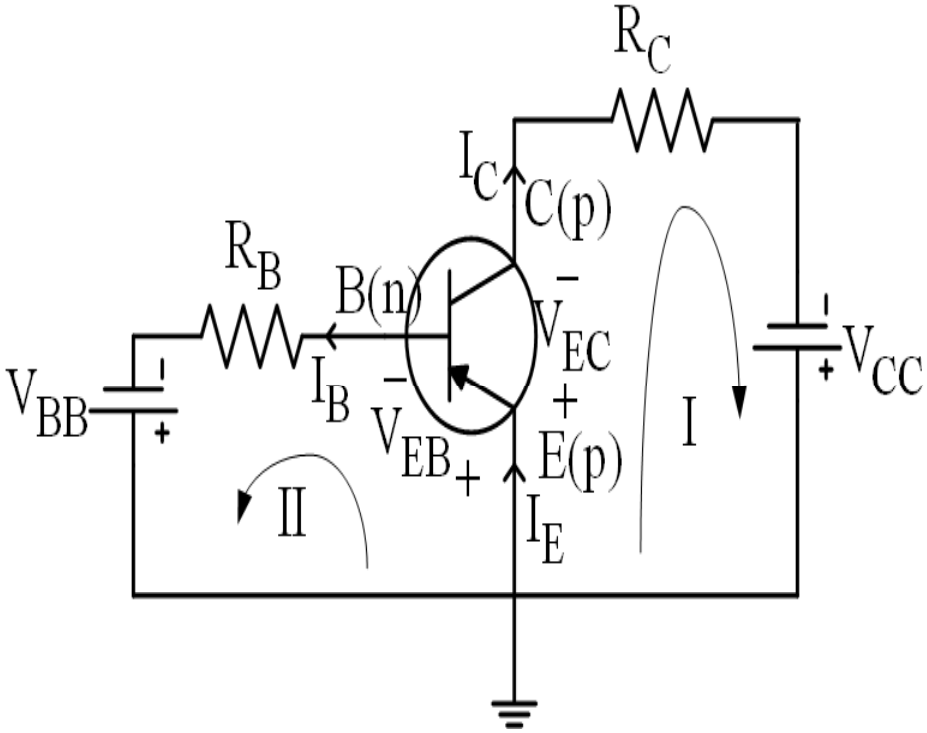
KVL for loop II:

$V_{EB} + I_B R_B - V_{BB} = 0$

$V_{EB} + I_B R_B = V_{BB}$

$I_B = (V_{BB} - V_{EB}) / R_B$

Since V_{BB} , V_{EB} and R_B are fixed, I_B is also fixed.



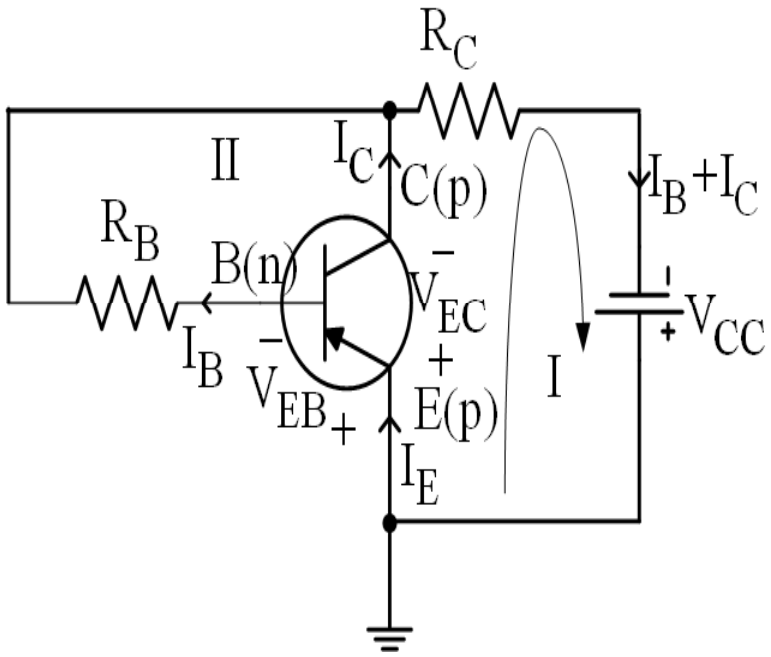
COLLECTOR TO BASE / COLLECTOR FEEDBACK BIASING CIRCUIT

KVL of loop I:

$V_{EC} + (I_B+I_C)R_C - V_{CC} = 0$

$V_{EC} + (I_B+I_C)R_C = V_{CC}$

$V_{EC} + (I_B+\beta_{DC}I_B)R_C = V_{CC}$ **if the minority carrier leakage current is neglected.**



KVL of loop II:

$V_{EB} + I_BR_B - V_{EC} = 0$

$I_B = (V_{EC} - V_{EB}) / R_B$

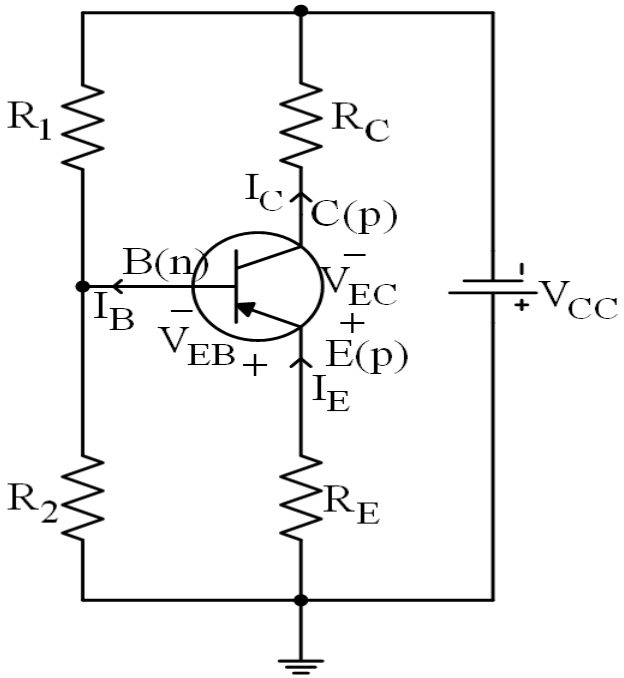
VOLTAGE DIVISION BIASING CIRCUIT

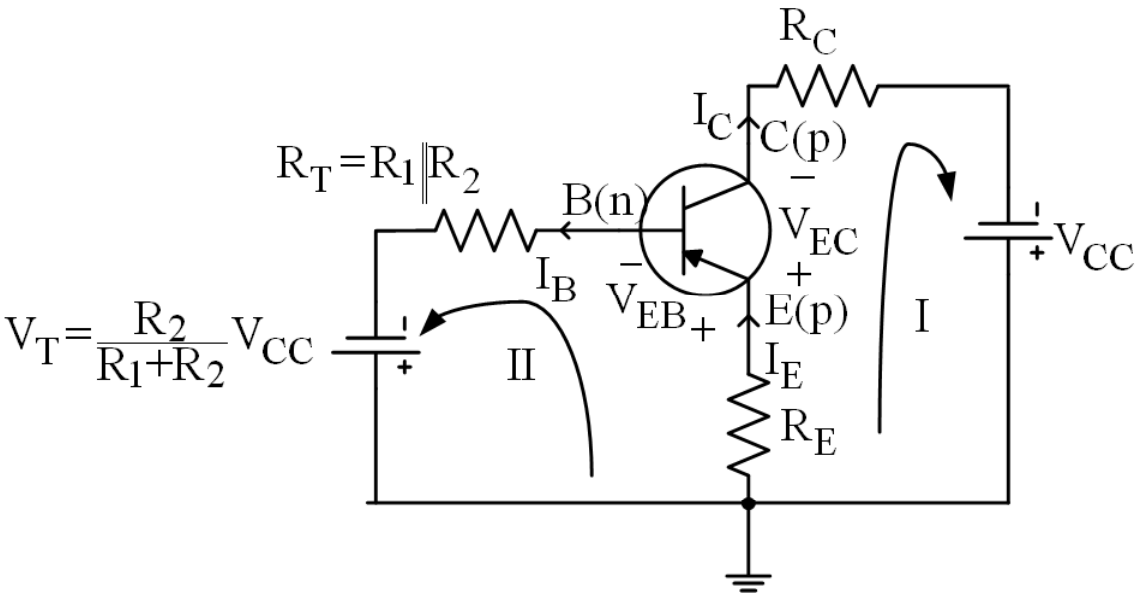
KVL of loop I:

$$I_E R_E + V_{EC} + I_C R_C - V_{CC} = 0$$

KVL of loop II:

$$I_E R_E + V_{EB} + I_B R_T - V_T = 0$$





STABILITY OF THE BIASING CIRCUITS

KVL for loop I:

$V_{EC} + I_C R_C - V_{CC} = 0$

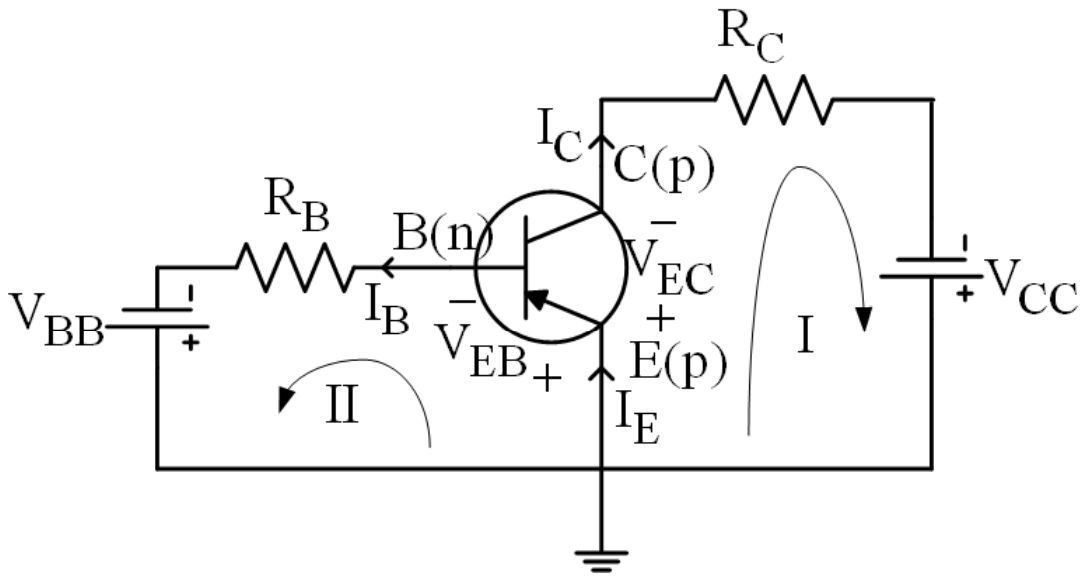
$V_{EC} + I_C R_C = V_{CC}$

KVL for loop II:

$V_{EB} + I_B R_B - V_{BB} = 0$

$V_{EB} + I_B R_B = V_{BB}$

$I_B = (V_{BB} - V_{EB}) / R_B$



Since V_{BB} , V_{EB} and R_B are fixed, I_B is also fixed.

If T↑, I_C↑ ; hence, V_{EC}↓. The Q point will change as the Q point of the CE circuit is I_{CQ} and V_{ECQ} .

As the I_B is fixed, this condition does not help in stabilizing the Q point of the circuit when changes occur. Thus, fixed-current biasing circuit is said to be less stable in terms of its biasing performance.

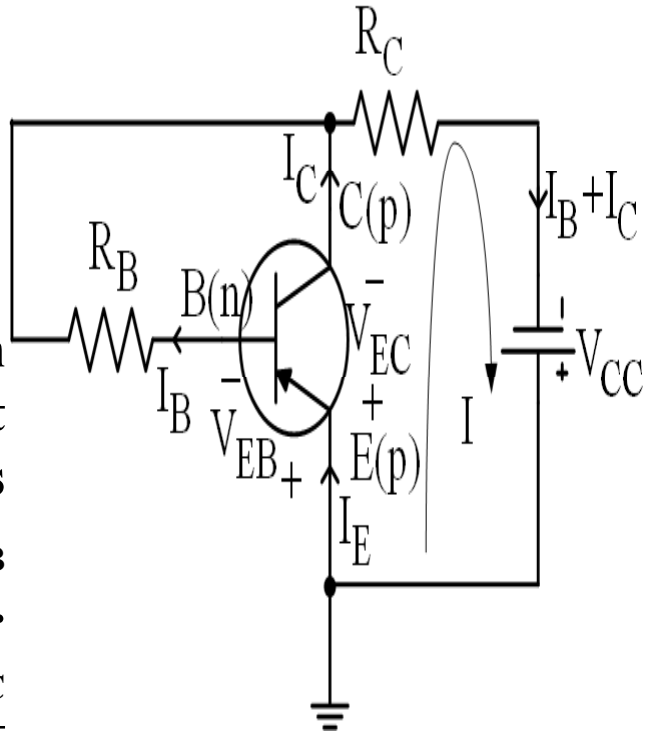
KVL of loop I:

$V_{EC} + (I_B+I_C)R_C = V_{CC}$ (1)

KVL of loop II:

$I_B = (V_{EC} - V_{EB}) / R_B$ (2)

From $I_C = \beta_{DC} I_B + I_{CEO}$, T↑ then I_C↑. From (1), V_{EC}↓ when I_C↑. If this happens, the Q point will change as the Q point of the CE circuit is I_{CQ} and V_{ECQ}. However, from (2), since V_{EB} and R_B are fixed values, I_B will ↓when V_{EC}↓. This condition will maintain the $(I_B+I_C)R_C$ term in (1). Hence, V_{EC} will be maintained at the quiescent value before the temperature change. Thus, collector feedback biasing circuit is said to be more stable in terms of its biasing performance.



KVL of loop I:

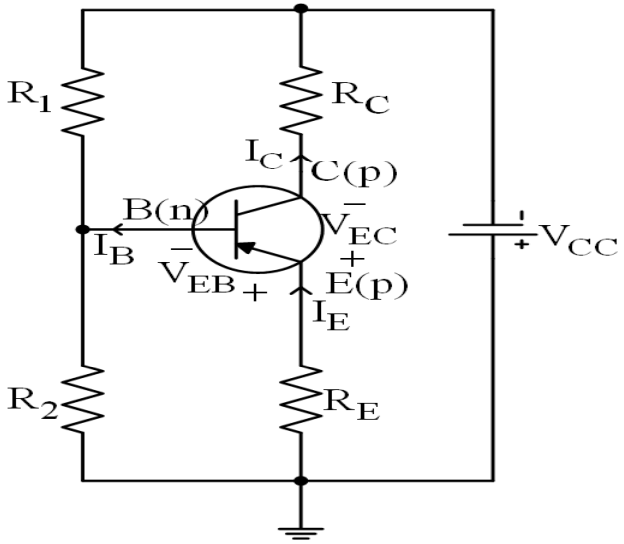
$$I_E R_E + V_{EC} + I_C R_C = V_{CC} \qquad (1)$$

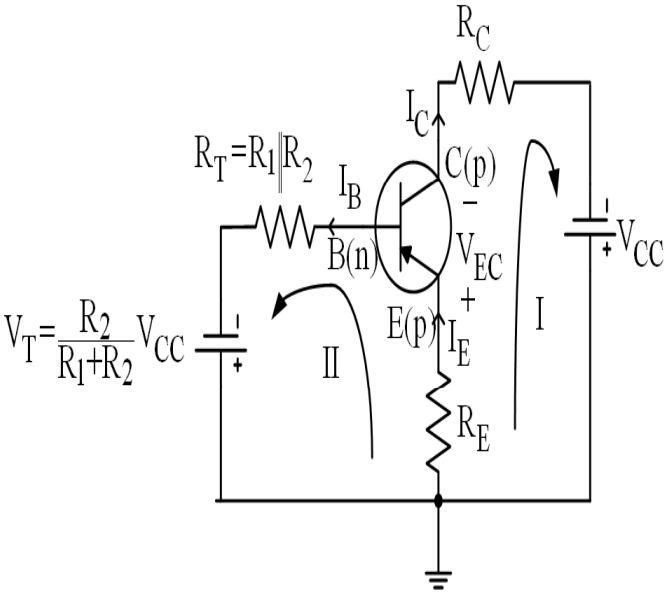
KVL of loop II:

$$I_E R_E + V_{EB} + I_B R_T = V_T$$

$$I_E R_E + I_B R_T = V_T - V_{EB} \qquad (2)$$

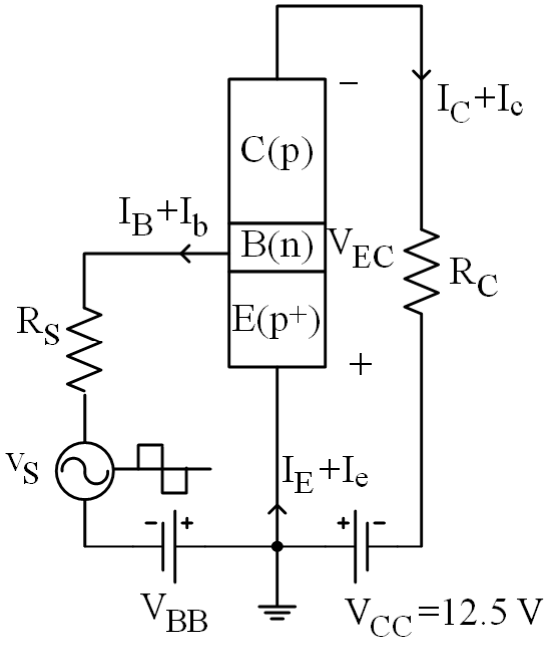
When T↑, then I_C↑. I_E will also ↑ as $I_C \approx \alpha I_E$. From (2), since V_{EB}, V_T, R_E and R_T are fixed values, when I_E↑, then I_B↓. From $I_C = \beta_{DC} I_B + I_{CEO}$, when T↑ I_{CEO} ↑ and will supposedly increase the I_C and consequently I_E However, this will make I_B↓. Thus, I_C will be maintained. Therefore, I_B is helping to stabilize the circuit by maintaining the Q point. This circuit is the most popular amongst the 3 biasing circuits discussed.

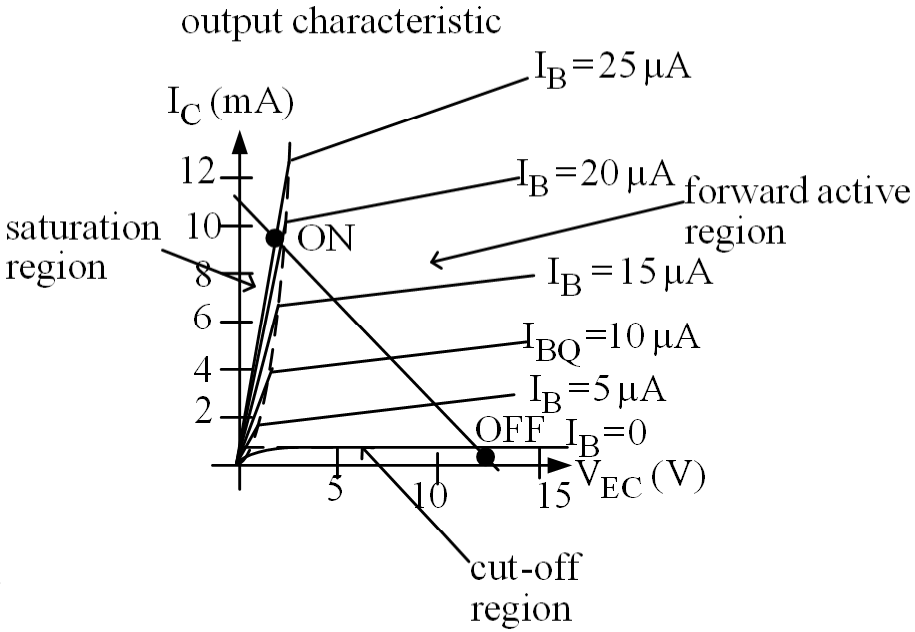




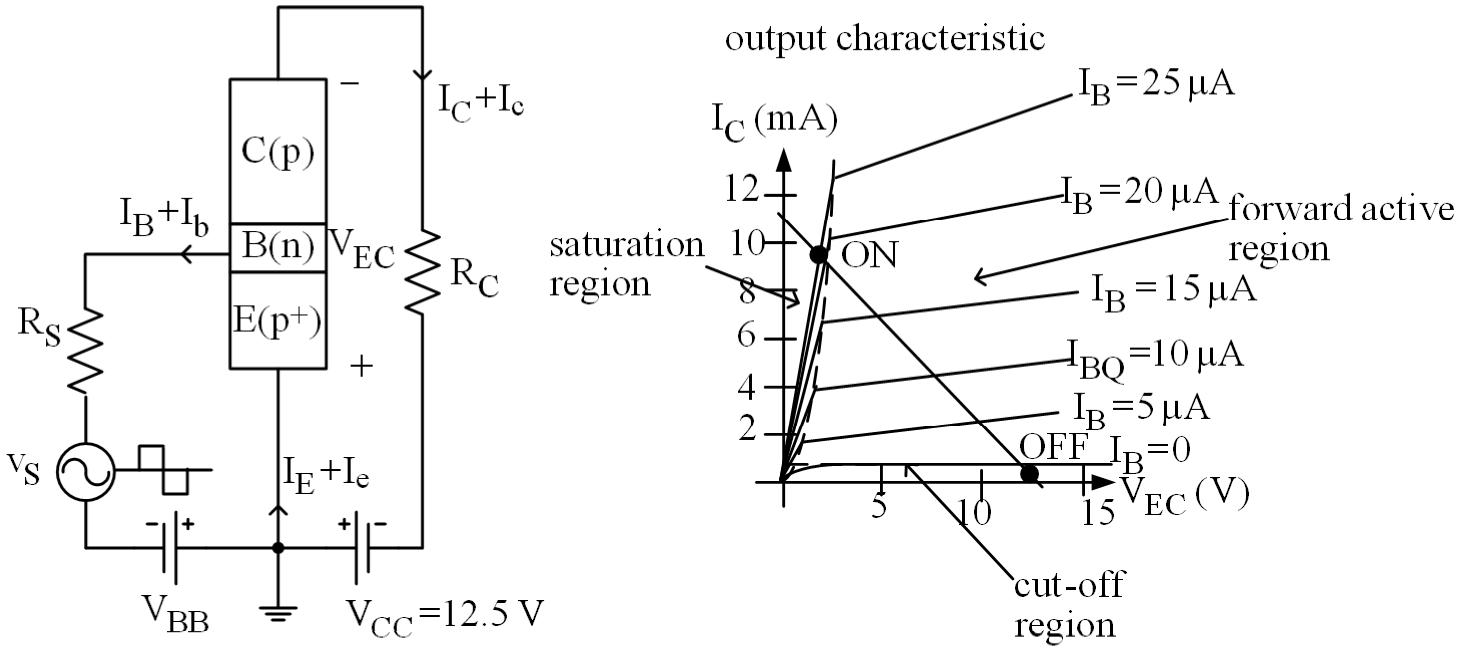
BJT AS A SWITCH

- **In digital applications, the transistors are normally utilized as switches. As a switch, I_B is used to convert I_C from OFF to ON.**
- **OFF condition: high voltage and low current**
- **ON condition: low voltage and high current**



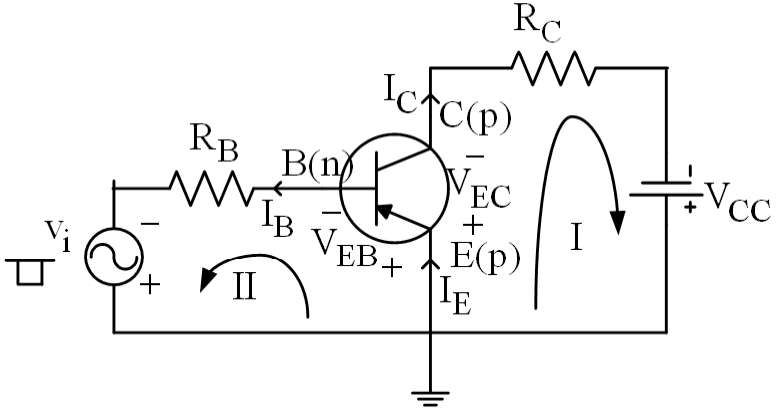


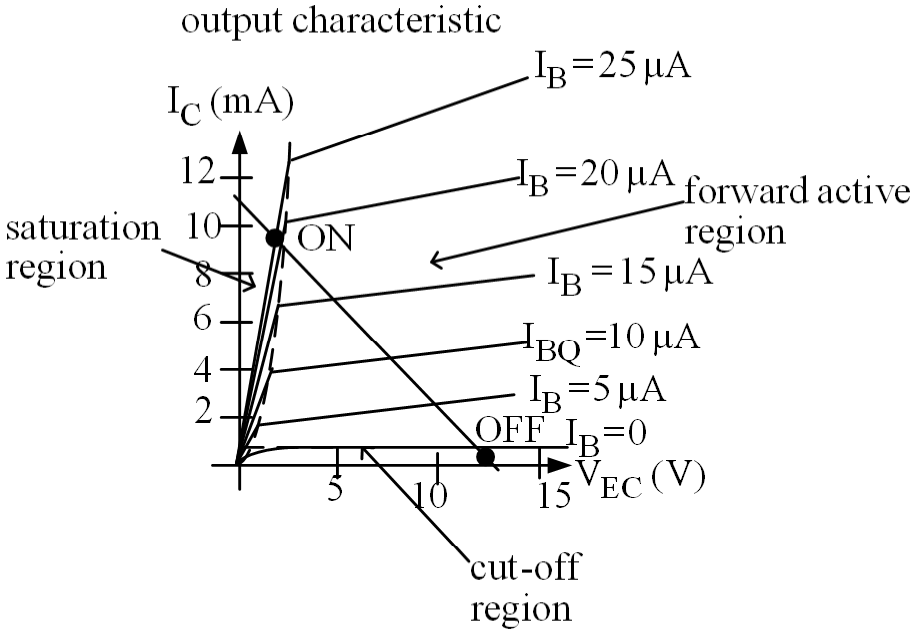
- **Transistor is an o/c between E and C in the OFF condition.**
- **Transistor is a s/c between E and C in the ON condition.**
- **Hence, the transistor's operation is like a switch.**



CUT-OFF

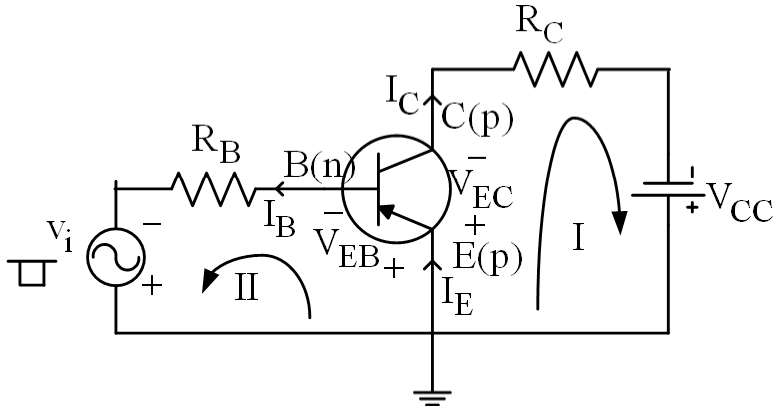
- **If $|v_i|$ is < 0.7, the E-B junction will let only a very small insignificant current to flow. Under this condition, the E-B junction is still considered as OFF. $I_B = I_C = I_E \approx 0$. $V_{EC} = V_{CC}$. B-C junction is also rb. The transistor is said to be in the cut-off condition (voltage is high, current is very small).**

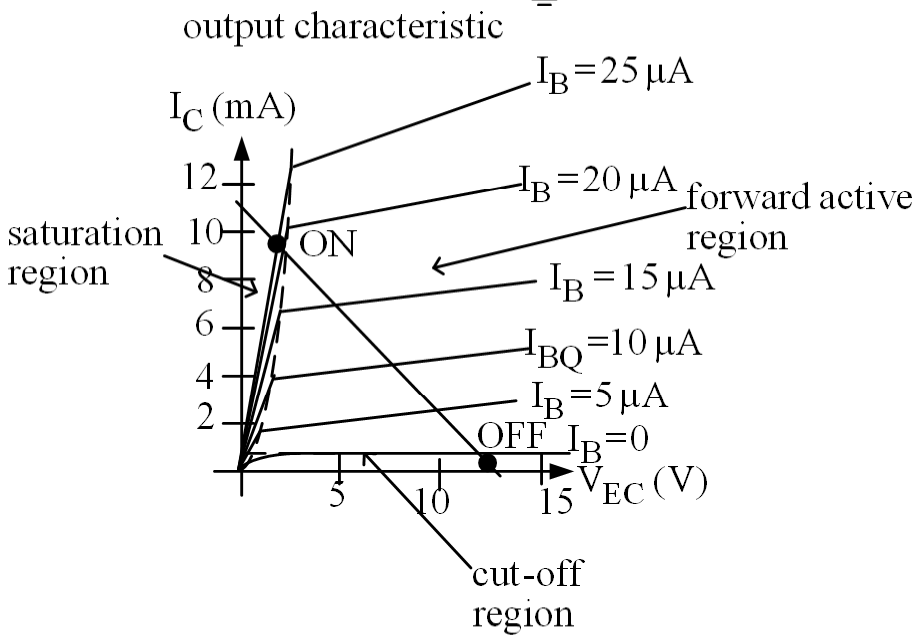




SATURATION

- **If $|v_i| \uparrow$, $I_B \uparrow$ $I_C \uparrow$ and $V_{EC} \downarrow$ (from $V_{EC} + I_C R_C = V_{CC}$). If the $|V_{EC}| < 0.7$ V, the device will enter the saturation region as both E-B and B-C junctions are fb.**
- **Under this condition, $|V_C| < |V_B|$. The B-C junction will be fb as the C is more +ve than the B. The B-C junction can be fb by a forward voltage of 0.4 to 0.5 V. The forward voltage drop of the B-C junction is smaller than the forward voltage drop of the E-B junction (i.e. 0.7 V) because C is doped less than E. [$V_o=(kT/q)\ln(N_A N_D/n_i^2)$].**

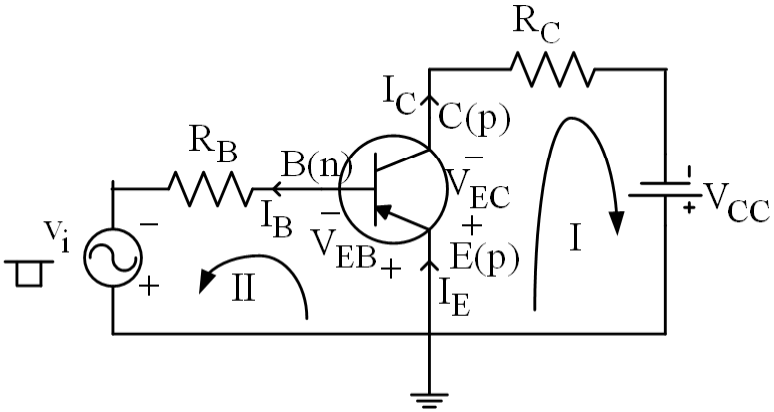


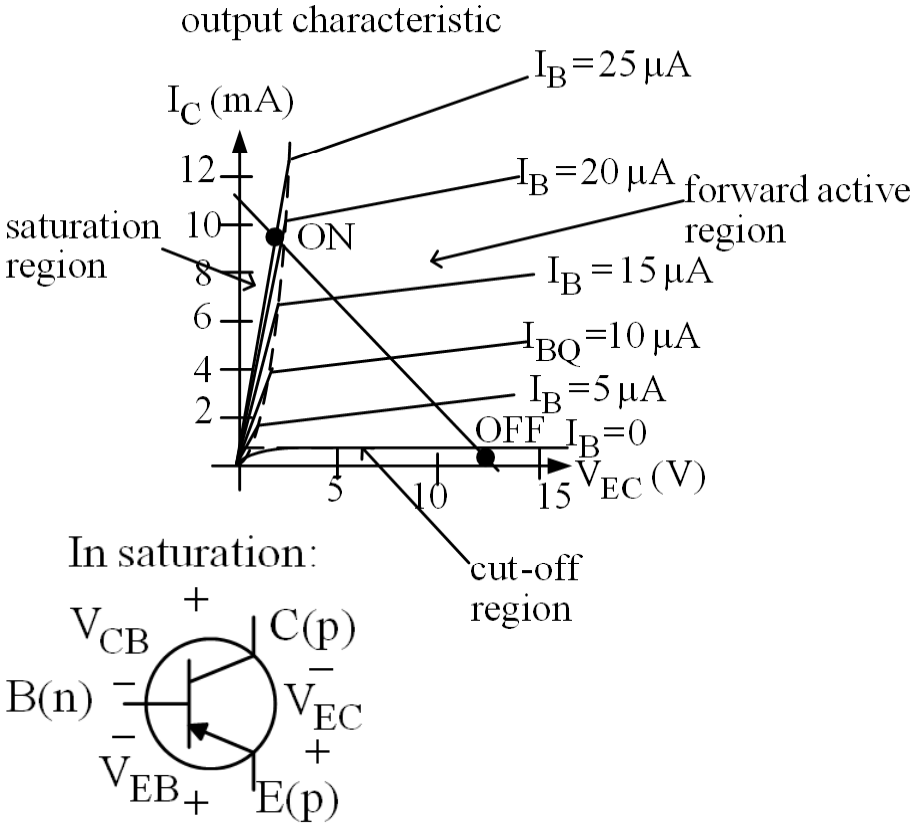


- **This condition is called saturation as any increment in the I_B will only cause the I_C to increase by a small amount and therefore, V_{EC} will also decrease by a small amount.**
- **The minimum rb of the BC junction is when $V_{BC} = 0$.**
- **In the saturation region, $\Delta I_C/\Delta I_B \neq \beta_{DC}$.**
- **As the forward voltage drop of the B-C junction is in the range 0.4 V to 0.5 V, then**

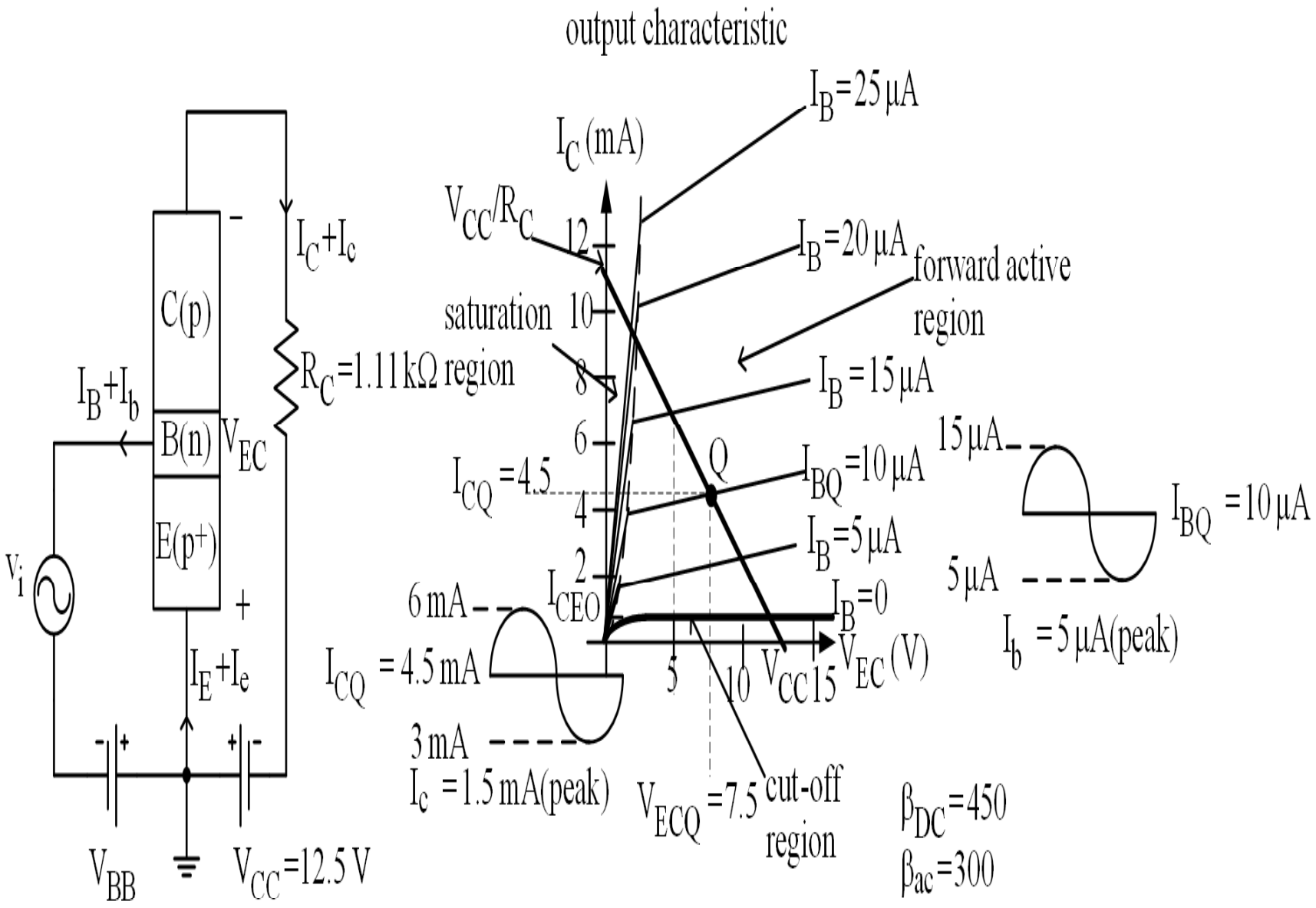
  $V_{EB} - V_{CB} - V_{EC} = 0$. Under this condition, $V_{EC} = V_{EC(sat)} = 0.3$ V to 0.2 V.
- **$V_{CC} = V_{EC(sat)} + I_{C(sat)}R_C$**

  $I_{C(sat)} = [V_{CC} - V_{EC(sat)}]/R_C$



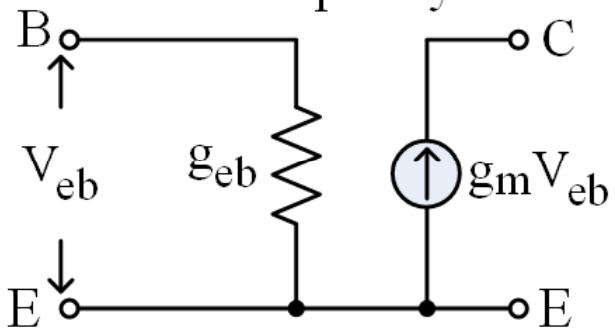


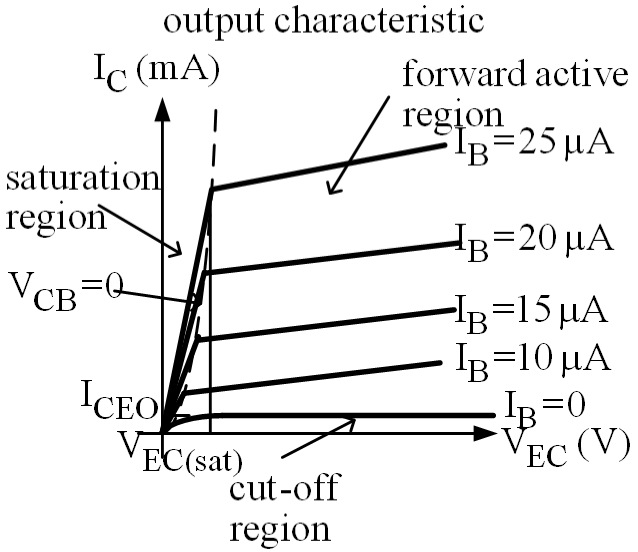
- **BJT has 4 modes of operation, i.e. forward active, saturation, cut-off and inverted. The mode of operation is dependent on the biasing condition of the BE and BC junctions.**
- **In analogue circuits, transistors normally operate in the active mode.**
- **In digital circuits, all 4 modes might be involved.**
- **So far, we had seen the static (or DC) characteristics of the BJT. Now we will learn about the AC characteristics of the BJT when a small-signal voltage or current is superimposed on its DC signal. Small-signal means the peak AC voltage and current are smaller than their DC values.**


output characteristic
I_C (mA)
V_{CC}/R_C
12
10
8
6
4
2
saturation region
forward active region
cut-off region
I_B=25 μA
I_B=20 μA
I_B=15 μA
I_B=10 μA
I_B=5 μA
I_B=0
Q
I_{CQ} =4.5
I_{CEO}
V_{ECQ} =7.5
5
10
V_{CC} 15
V_{EC} (V)
6 mA
I_{CQ} = 4.5 mA
3 mA
I_c =1.5 mA(peak)
15 μA
5 μA
I_{BQ} =10 μA
I_b =5 μA(peak)
β_{DC}=450
β_{ac}=300
C(p)
B(n)
E(p+)
I_C+I_c
R_C=1.11 kΩ
I_B+I_b
V_{EC}
I_E+I_e
V_i
V_{BB}
V_{CC}=12.5 V

SMALL-SIGNAL EQUIVALENT CIRCUIT OF BJT

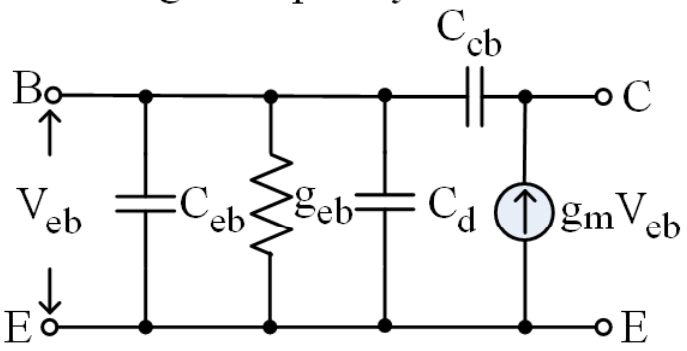
Basic equivalent circuit for low-frequency





- **$g_m = I_c/V_{eb}$ is the transconductance.**
- **$g_{eb} = I_b/V_{eb}$ is the i/p conductance. This conductance must be included as we are considering the current that is flowing through the fb E-B junction.**
- **At higher frequencies, when E-B is fb, there exist a depletion capacitance, C_{eb}, and diffusion capacitance, C_d. For the rb B-C junction, there exist only the depletion capacitance, C_{cb}.**

Basic equivalent circuit for high-frequency



Depletion capacitance:

Independent of whether the junction is forward or reverse biased, there exist the depletion region on both sides of the junction. The p-depletion region-n structure is similar to the structure of the capacitor. Due to the depletion region, depletion capacitance, C_j, exist.

$C_j = dQ/dV = dQ/(WdQ/\varepsilon A) = \varepsilon A/W$
(unit for C_j is F/cm^2)

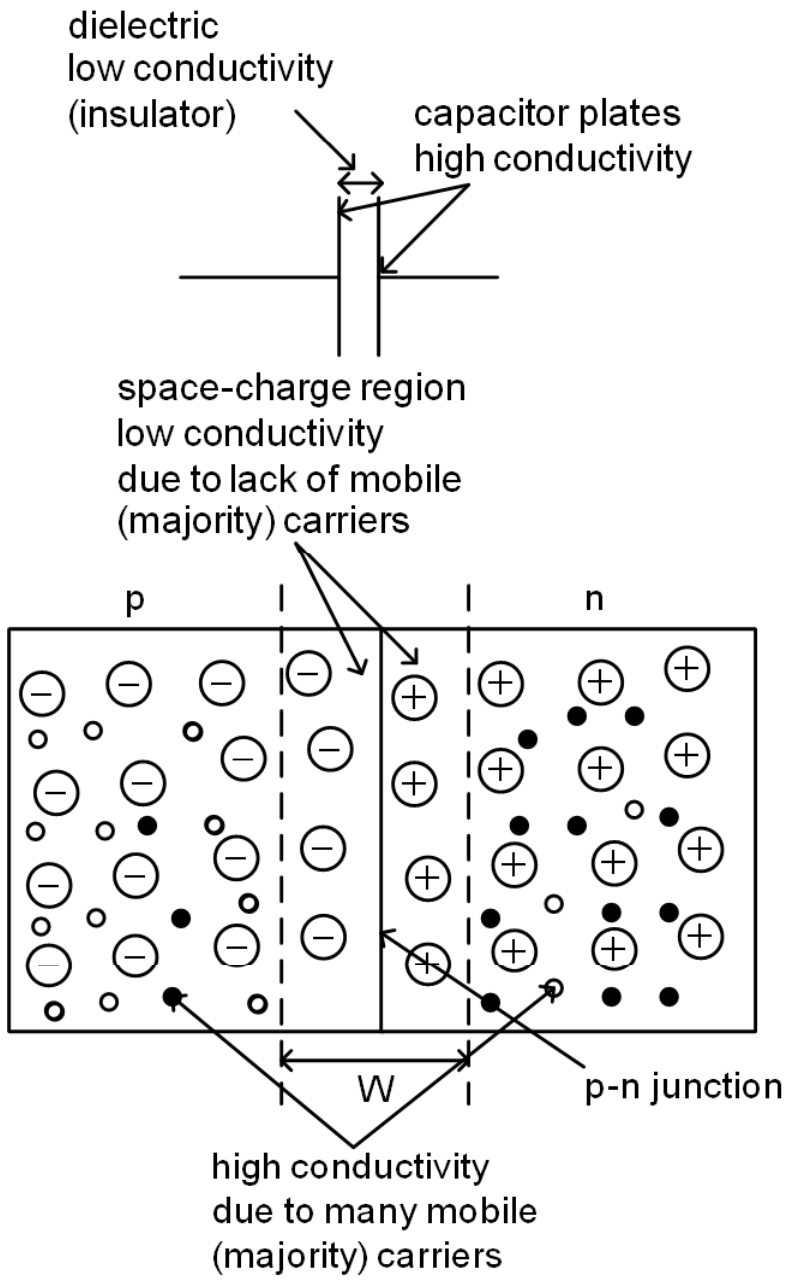
dQ = change of charge per unit area of the depletion layer.

dV = change of voltage applied.

A = cross-section area.

ε = permittivity of Si

W = width of the depletion region



Diffusion capacitance

- **When the p-n junction is fb, large current flows through the junction. This will result in many mobile carriers to be in the neutral B. The change in the mobile carriers corresponding to the change in the biasing voltage will result in the diffusion capacitance, C_d.**
- **$C_d = (Aq^2L_pp_{no}/kT)e^{qV/(kT)}$**

  where

  L_p = diffusion length of hole in the n material

  p_{no} = equilibrium hole density in the n